Development and performance evaluation of a chip-based liquid juction nanoelectrospray CE-MS interface

Lukas Naumann, Aalen University

Capillary electrophoresis (CE) coupled with mass spectrometry (MS) results in a very fast and efficient separation technique, which can detect numerous analytes at the same time. The dilution factor of the conventional Triple-Tube coaxial sheath-flow interface (TTS), leads to a loss of sensitivity compared to GC-MS and LC-MS approaches. Therefore, Agilent investigates a novel chip-based liquid junction nanoESI CE-MS interface with a 50fold decreased liquid flow rate compared to the TTS. So, the new chip interface should have less analyte dilution and probably a higher sensitivity.

Within this Master Thesis, the performance of the novel chip-based liquid junction nanoESI CE-MS interface was examined. A new source prototype for the in-line setup was developed and manufactured. During the research work, a lot of troubleshooting had to be done, because all the new chips were blocked, due to problems during the manufacturing process. Despite these difficulties, it was possible to perform a parameter optimization for the in-line setup with the new source prototype with a design-of-experiment (DoE) approach. For the performance evaluation of the chip interface a limit-of-detection (LOD) determination was performed with the TTS in two operation modes (with/without nebulizing gas). The performance evaluation shows that the TTS without nebulizing gas performs in the same order of magnitude like the chip in-line set-up. Because of the extrapolation of the SNR respectively LOD from the DoE confirmation experiments, the results obtained with the chip interface must be critically viewed. Also, the measurement-to-measurement repeatability is not optimal with these used chips.

The chip-to-chip derivation can't be shown in this thesis, caused by a low available number of working chips. A fine working CE-MS chip production in the future is highly improbable, because of the end-of-life state of the chip-cube interface. If in the future there are some working chip available, robustness testing, chip-to-chip variability, long term stability (erosion, blockage, corona discharge) and LOD measurement series could be performed. Another interesting parameter which can be investigated is the chips ohmic resistance. If this parameter decreases, the chip is close to the end of his life. A new approach for the chip

manufacturing could be also tested, like 3D-printed chips. The main disadvantage of the 3D printing process is the size limitation of the printers.